DESIGN CONSIDERATIONS OF ACTIVE ELEMENT ARRAY TRANSCEIVERS

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Abstract

Mechanical and electrical design considerations, including performance trade-offs of microwave integrated circuit solid state active element array transceiver modules operating in the L-Band region will be presented.

In examining the decisions that are made in the design of active element array transceivers, it is helpful to make reference to a block diagram, such as Figure 1. The first component encountered in the receiver's signal path is the 3-port circulator. The circulator requirements are small size, light weight, low insertion loss (over some specified temperature range), moderate isolation and VSWR. The circulator depicted in Figure 2 is one (1) inch square by 1/4 inch thick with the weight slightly less than one (1) ounce. The design specifications, therefore, dictate the use of an above-resonance circulator with appropriate temperature compensation.

The next component in the receive path performs a front-end protection function, i.e., protection of the succeeding receiver elements against damage from excessive power levels. The protect function in the particular case illustrated here, is provided by a single-pole, double-throw switch, cascaded with a diode limiter. The SPDT switch in this case, is TTL compatible and uses a minimal amount of bias current while maintaining a low insertion loss. Normally, the transceiver module efficiency is an important consideration which provides the motivation for using small bias current, as well as accounting for the obvious TTL current sinking limitations.

The next component to be considered is the low noise amplifier where there are many design decisions to be made. The selection of transistors and their operating conditions influences the system noise figure, gain and gain compression and as such, are subjected to very careful analysis. In a phased array application, the amplifier must be phase and amplitude stable with variation in supply voltages, temperature, etc., which encourages the use of active bias schemes as a means of providing the required stability. A constant group delay and a specified insertion phase imposes rigid criteria on the interstage coupling structures. Yet another consideration is the inter-relationship between source impedance, amplifier noise figure and the resulting input VSWR. The load sensitivity of the amplifier may be alleviated with moderate padding provided there is adequate gain margin. Several computer optimization programs exist to assist with the initial design.

The T/R switch performs the function indicated by its name, allowing the manifold port to operate either as an input or an output. The switch is interfaced with TTL logic as it is in the case of the front-end protection switch. The T/R switch diode current must also be held to a minimum for identical reasons. The switching speed and related requirements are the most frequently encountered design considerations.

Another key component and one which is often the subject of extensive design effort is the phase shifter. The type illustrated in Figure 3 is the 4-bit Switched Line variety. The placement of the bias lines, the diode spacing, sequence and other parameters are best determined by successive iterations of a circuit analysis program (or a network optimization program). Some of the important considerations in the design of the phase shifter are: stability with temperature and voltage supply variations, linear phase change versus frequency, minimum phase settling time and diode current. The phase shifter described here is also TTL compatible and consequently maintaining a low diode current is mandatory since eight (8) diodes must be forward biased to the "ON" state.

The transmitter frequently has a Class "A" state input to permit operation at low input power levels. When space and weight allocations are adequate, it can be preferrable to use a balanced technique which affords improved input VSWR performance. The balanced amplifier also provides a relatively constant source impedance to the Class "C" power amplifier which follows as well as a constant load impedance to the phase shifter. The remainder of the transmitter incorporates four cascaded common base transistor stages operating Class "C" to achieve a minimum power output of 120 watts over a 10% bandwidth with 30 dB of gain. The high-power bandwidth product is achieved through the use of "Ampac", internally matched transistors in the output stages. The photo of Figure 4 indicates the implementation of this technique. Power combination in the output stages is by means of interdigital quadrature couplers for wide bandwidth, minimum area and low loss. Driver stages are designed utilizing impedance transforming low pass filter structures. The optimization provides the bandwidth and gain required.

Of particular interest is the pulse performance achieved over a rather wide range of pulse widths and duty cycles. Those results described in Table 1 are the average of eight amplifiers. In an amplifier of this type, pulse shape is a function of the dc bias circuit, and the RF bandwidth. Since the bandwidth is over 200 MHz, the rise-time contribution of the tuned circuits is less than 1.5 nsec. Of much greater importance is the inductance of leads to the energy storage capacitor. To minimize this effect, two 250 μf capacitors are mounted on the amplifier and the runs kept as short as possible to the output devices. The blocking chokes are chosen as small as possible, consistent with RF isolation. Careful consideration is also given to the emitter return circuits to minimize rise-time.

Another characteristic of primary importance in an array module, is phase control. Table II describes the results of this module. To achieve this level of performance requires particular attention to stage efficiencies, since these affect AM/PM conversion and intrapulse phase variation. These variations are caused by heating in the device, thereby causing variations in transit time. By keeping efficiency high, heating is minimized and phase shifts kept small.

A further benefit of high stage efficiency is maintenance of low junction temperatures and thereby improved MTBF. Table III indicates the calculated junction temperatures of the amplifier chain.

TABLE I
POWER OUTPUT PERFORMANCE

	FREQ	100 μs, 1%		100 μs, 10%		500 μs, 10%	
		Po(W)	eff(%)	Po(W)	eff(5)	Po(W)	eff(%)
	f_o - 5%	142	(39.4)	139	(39.3)	131	(39.2)
Average	f_o	140	(38.0)	135	(37.6)	129	(36.7)
	f_o + 5%	125	(38.2)	124	(38.0)	119	(37.1)

TABLE II
PHASE PERFORMANCE @ 100 μs, 10% D.F.

FREQ	Intrapulse Φ Linearity	AM/PM Deg/dB	$\Delta\Phi/\Delta$V Deg/Volt	$\Delta\Phi$ / ΔT Deg/Deg C
f_o - 5%	3.3	4.0	3.1	---
f_o	3.5	4.6	2.5	.26
f_o + 5%	4.1	4.9	1.8	---

TABLE III
PEAK JUNCTION TEMPERATURES OF OUTPUT & DRIVER STAGES

STAGE	T, @ 30°C CASE	Max θ_j (°c/w)
Output (1213-40)	97°C	2.25
Driver (1315-3)	106°C	7

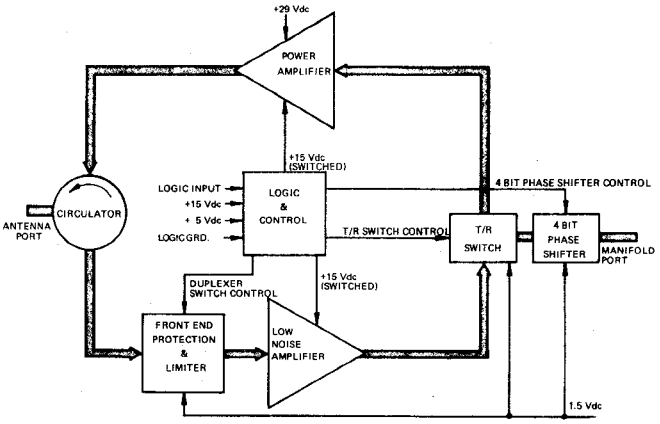

FIGURE 1 FUNCTIONAL SYSTEM BLOCK DIAGRAM

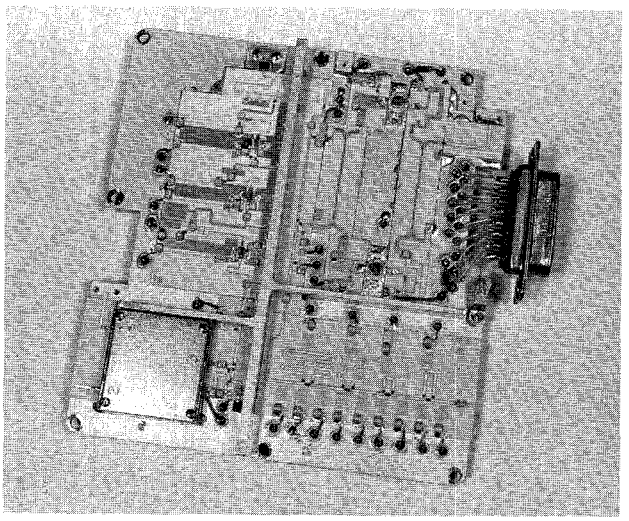

FIGURE 2 RECEIVER PORTION OF TRANSCEIVER

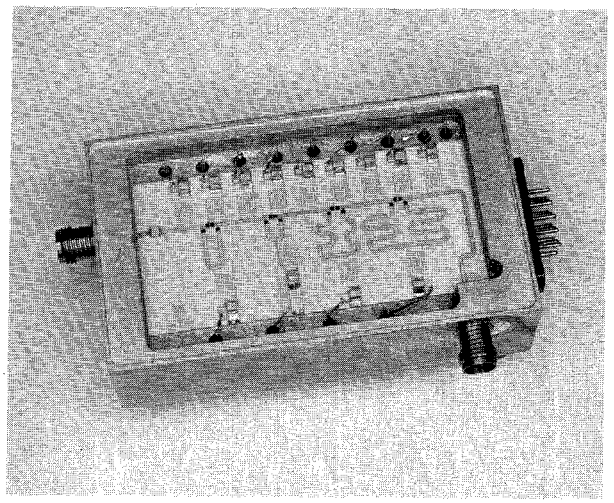

FIGURE 3 FOUR BIT SWITCHED LINE PHASE SHIFTER

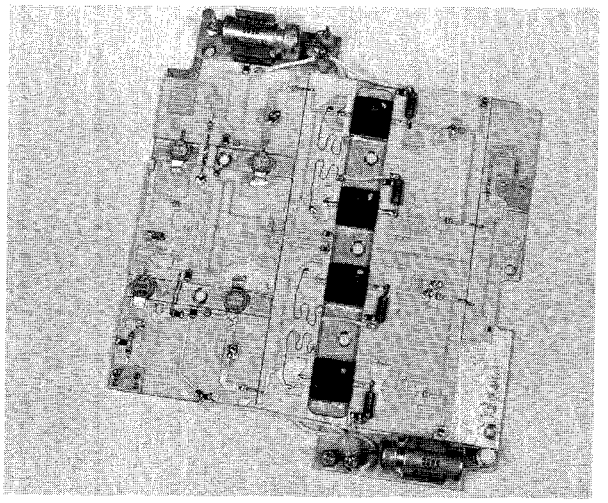

FIGURE 4 TRANSMITTER PORTION OF TRANSCEIVER